

60V N-Channel Power MOSFET

• **General Description**

It combines trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

• **Features**

- AEC-Q101 Qualified
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

• **Application**

- BLDC Motor driver
- DC-DC
- Battery protection

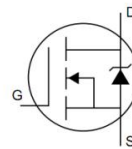
• **Ordering Information:**

Part NO.	ZMA430N06U
Marking	430N06
Packing Information	REEL TAPE
Basic ordering unit (pcs)	3000

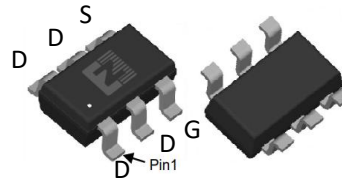
• **Absolute Maximum Ratings** ($T_C=25^{\circ}\text{C}$)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		60	V
Gate-Source Voltage	V_{GS}		± 20	V
Continuous Drain Current	I_D	$T_C=25^{\circ}\text{C}$	3.1	A
	I_D	$T_C=75^{\circ}\text{C}$	2.4	A
	I_D	$T_C=100^{\circ}\text{C}$	2.0	A
Pulsed Drain Current	I_{DM}	Pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25^{\circ}\text{C}$;	12.4	A
Total Power Dissipation	P_D	$T_C=25^{\circ}\text{C}$	5	W
Total Power Dissipation	P_D	$T_A=25^{\circ}\text{C}$	0.7	W
Operating Junction Temperature	T_J		-55 to +150	$^{\circ}\text{C}$
Storage Temperature	T_{STG}		-55 to +150	$^{\circ}\text{C}$
Single Pulse Avalanche Energy	E_{AS}	$L=0.1\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	5	mJ
		$L=0.5\text{mH}$, $V_{GS}=10\text{V}$, $R_g=25\Omega$,	10.5	mJ
ESD Level (HBM)	CLASS 1B			

• **Product Summary**



$V_{DS} = 60\text{V}$
 $R_{DS(ON)} = 60\text{m}\Omega$
 $I_D = 3.1\text{A}$



SOT-23-6



•Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	25	°C/W
Thermal resistance, junction-ambient ^①	R_{thJA}		-	180	°C/W
Soldering temperature	Tsold		-	260	°C

•Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	1.3	1.7	2.5	V
Drain-Source Leakage Current	I_{DSS}	$V_{GS}=0V, V_{DS}=60V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=5A$		60	75	m Ω
		$V_{GS}=4.5V, I_D=3A$		70	90	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_{SD}=10A$		5		S
Diode Forward Voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=5A$			1.3	V

•Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1MHz, V_{DS}=25V$	-	715	-	pF
Output capacitance	C_{oss}		-	34	-	
Reverse transfer capacitance	C_{rss}		-	18	-	
Gate Resistance	R_g	$f=1MHz$	-	1		Ω
Total gate charge	Q_g	$V_{DD}=15V, I_D=20A, V_{GS}=10V$	-	10.6	-	nC
	$Q_g(4.5V)$		-	5.5	-	
Gate - Source charge	Q_{gs}		-	2.5	-	
Gate - Drain charge	Q_{gd}		-	1.5	-	
Turn-ON Delay time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=15V, R_G=3.3\Omega, I_D=20A$	-	2	-	ns
Turn-ON Rise time	t_r		-	3	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	10	-	ns
Turn-Off Fall time	t_f		-	7.5	-	ns
Reverse Recovery Time	t_{RR}	$V_{DD}=20V, dI_S/dt=100A/\mu s, I_S=20A$	-	29	-	ns
Reverse Recovery Charge	Q_{RR}		-	28	-	nC

Fig.1 Gate-Charge Characteristics

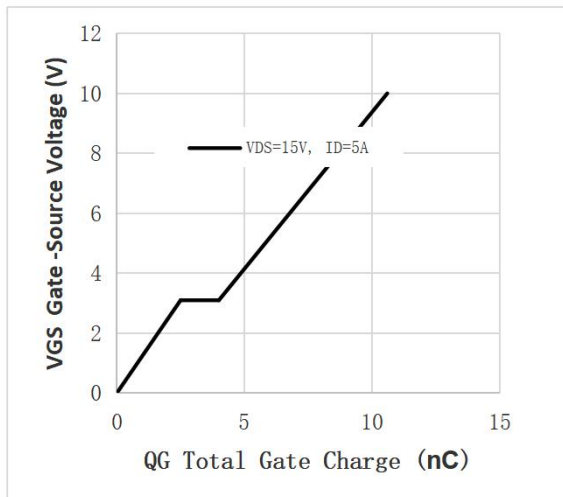


Fig.2 Capacitance Characteristics

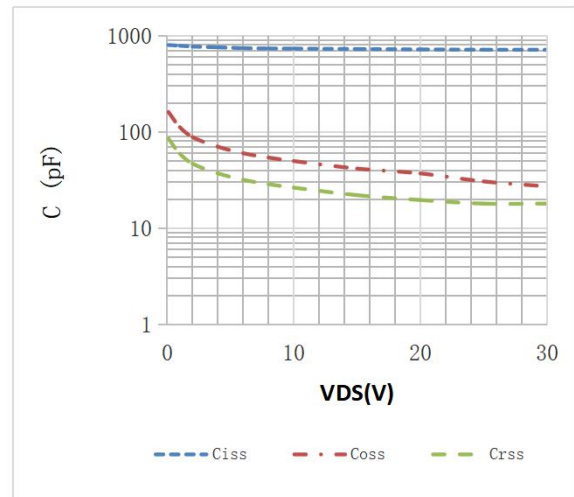


Fig.3 Power Dissipation

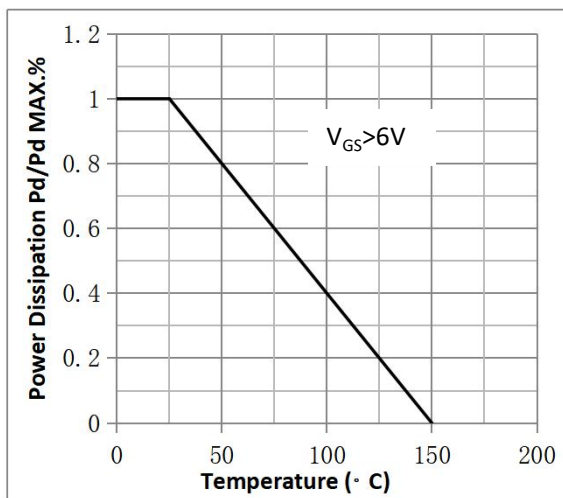


Fig.4 Typical output Characteristics

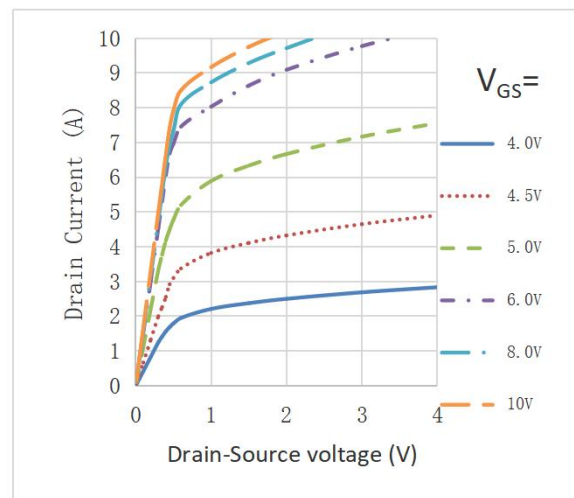


Fig.5 Threshold Voltage V.S Junction Temperature

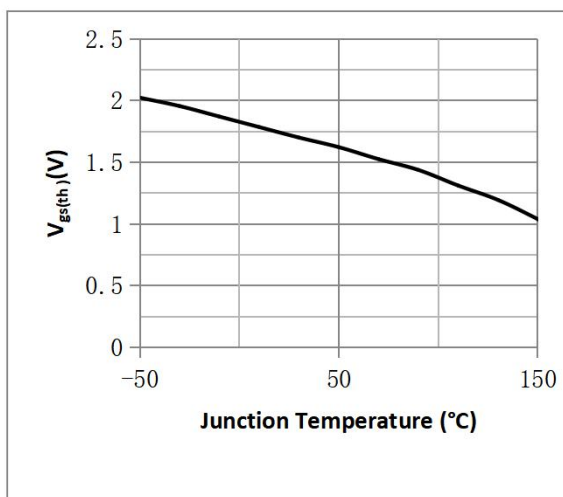


Fig.6 Resistance V.S Drain Current

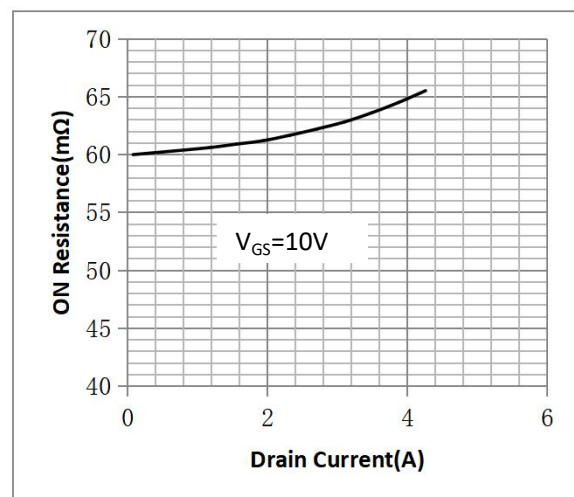


Fig.7 On-Resistance VS Gate Source Voltage

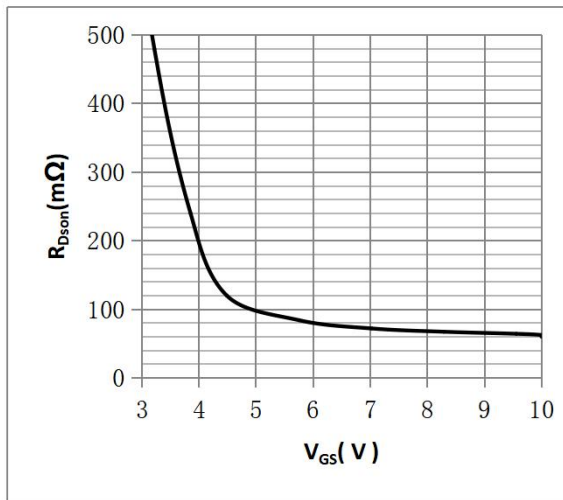


Fig.8 On-Resistance V.S Junction Temperature

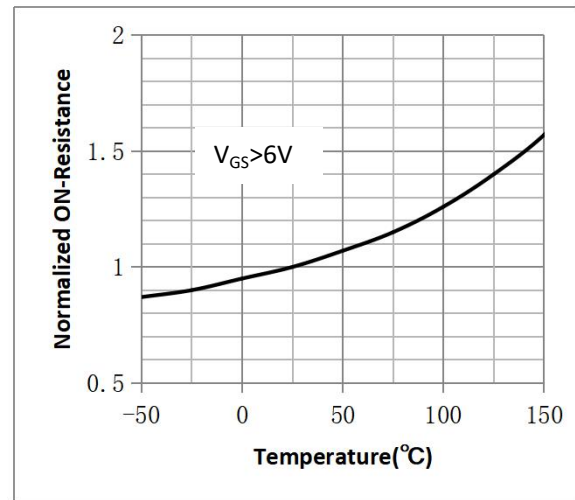


Figure 9. Diode Forward Voltage vs. Current

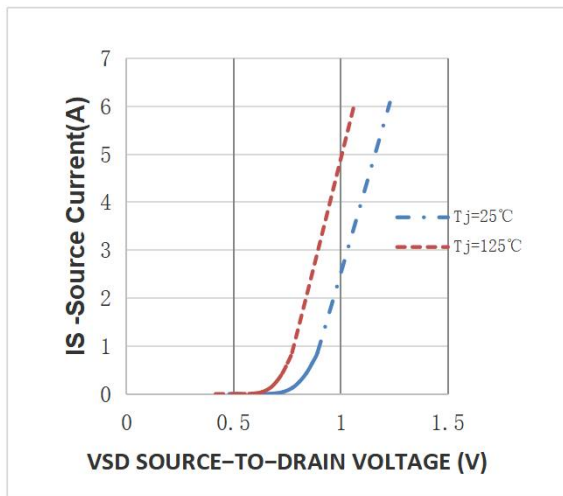


Figure 10. Transfer Characteristics

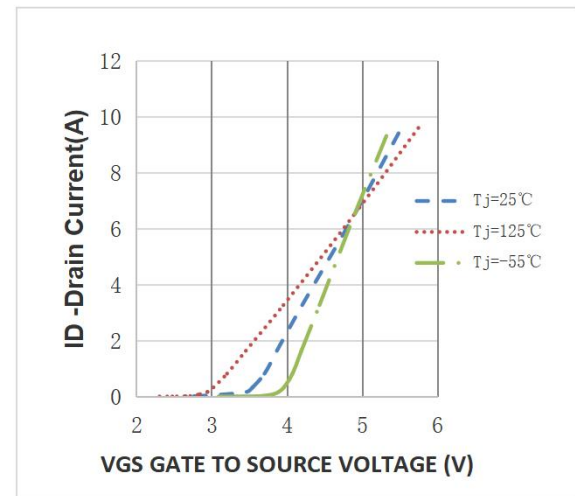


Fig.11 Safe Operating Area

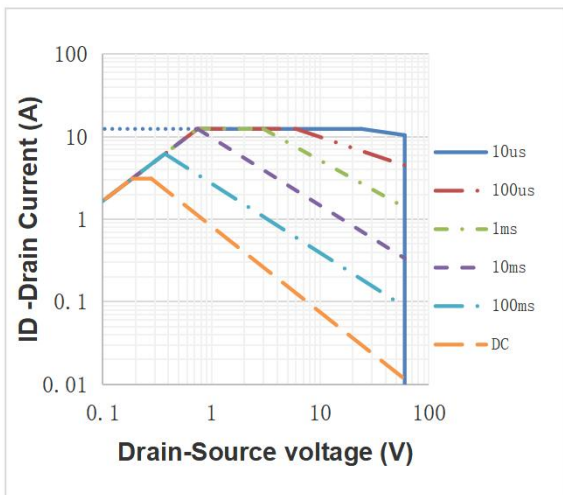
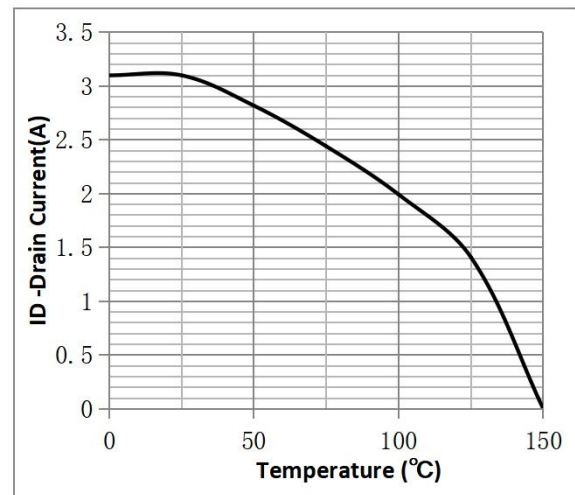
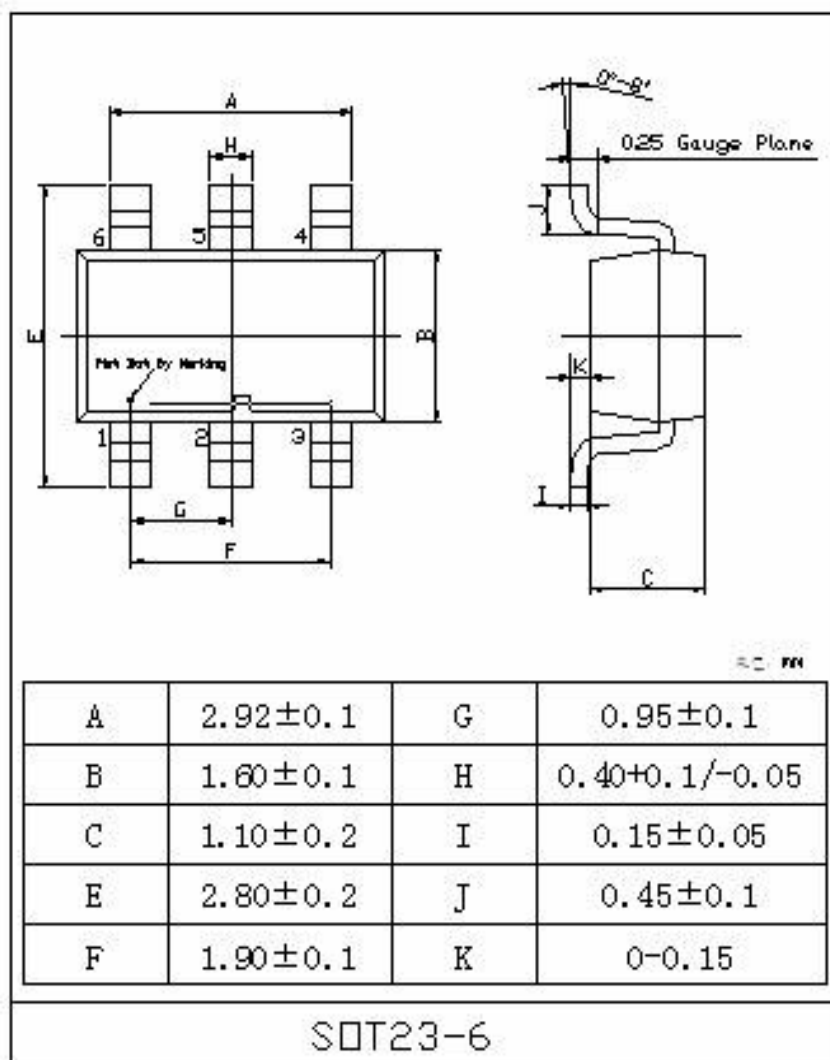


Fig.12 I_D vs. Case Temperature^②



•SOT-23-6 Package Outline





Note:

- ① Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ② Practically the current will be limited by PCB, thermal design and operating temperature. VGS=10V.

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Revision History

Version	Date	Change
A	2021.12.10	
B	2022.9.5	1.Add Reach, HF figure, 2.ID modify